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COMPUTATIONAL INTELLIGENCE, MAN- MACHINE SYSTEMS and CYBERNETICS

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COMPUTATIONAL INTELLIGENCE, MAN-MACHINE SYSTEMS and
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Electrical and Computer Engineering Series
A Series of Reference Books and Textbooks

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Preface

The book you are currently holding contains the Proceedings of the 6th WSEAS International Conference on COMPUTATIONAL INTELLIGENCE, MAN-MACHINE SYSTEMS and CYBERNETICS (CIMMACS '07) which was held in Puerto De La Cruz, Tenerife, Canary Islands, Spain, December 14-16, 2007

The CIMMACS'07 is the internationally recognized Forum for the dissemination of the latest advances on Neural Networks, Fuzzy Systems, Evolutionary Computation, Artificial Intelligence, Systems Theory, Man-Machine Systems, Cybernetics, Simulation, Modelling, Optimization etc as well as their impact and their interaction with other areas of Computer Science and Engineering. The various WSEAS conferences on Neural Networks, Fuzzy Systems, Evolutionary Computation, Artificial Intelligence, Systems Theory, Man-Machine Systems, Cybernetics, Simulation, Modelling, Optimization has been successfully held each year since 1996 and has produced more than 150 volumes of Proceedings while the best papers and the invited papers after extension and after peer review from 4 international referees, are published in WSEAS Journals covered by all the major scientific indexes.

The 6th WSEAS International Conference on CIMMACS'07 disseminated the latest research and applications in the afore mentioned fields. The friendliness and openness of the WSEAS conferences, adds to their ability to grow by constantly attracting young researchers.

The WSEAS International Conference CIMMACS'07 attracted a good number of well-established and leading researchers in the aforementioned areas as well as Modern and Advanced Applications in the Real Life. The CIMMACS always has a special appeal to young researchers and is characterized by a friendly atmosphere in which delegates at different stages of their careers can talk to each other. Scientists within the areas of Information Technologies will benefit from attending the meeting. As a conclusion, the conference offers to the engineers and scientists a unique forum for establishing new collaborations within present or upcoming research projects, exchanging useful ideas, presenting recent research results, participating in discussions and establishing new academic collaborations, linking university with the industry.

You can also attend other similar WSEAS conferences on Neural Networks, Fuzzy Systems, Evolutionary Computation, Artificial Intelligence, Systems Theory, Man-Machine Systems, Cybernetics, Simulation, Modelling, Optimization, Applied and Theoretical Informatics via: www.worldses.org/history.htm

We would like to address to each of you a warm invitation for the 7th WSEAS International Conference on ARTIFICIAL INTELLIGENCE, KNOWLEDGE ENGINEERING and DATA BASES (AIKED'08) (that will be held in the University of Cambridge) where our “father” Prof. **Lotfi A. Zadeh** will be for 4th time Plenary Speaker in a WSEAS Congress presenting the Plenary Lecture: “*Toward Human-Level Machine Intelligence*”. Details:

<http://www.wseas.org/conferences/2008/cambridge/aiked/Plenary1.htm>

The Plenary Speeches of CIMMACS'07 were:

Learning Data Structures with Inherent Complex Logic

Professor Wlodzislaw Duch

Dept. of Informatics, Nicolaus Copernicus University
Torun, Poland

Abstract: The greatest challenge for computational intelligence is to learn in difficult, highly non-separable situations. Current state-of-the-art learning algorithms are useful only when data is linearly separable using appropriate kernels. Even simple problems with non-trivial logic, like parity problems, cannot be learned with such algorithms. Many problems in bioinformatics and text analysis require complex logic or discovery of (approximate) logical structure in the data. Visualization of learning dynamics in neural networks shows that frequently separability cannot be achieved, but simpler goals for learning may be set. k -separability, or the projection of data on a line and segmentation into intervals, is an interesting concept that allows for estimation of the degree of non-separability. Difficult problems may be learned in this way although quite different algorithms are required.

Brief Biography of the Speaker:

Wlodzislaw Duch heads the Department of Informatics, Nicolaus Copernicus University, Torun, Poland, and is a Visting Professor at Nanyang Technological University, Singapore (2003-7). Ph.D. in quantum chemistry (1980), postdoc at USC, Los Angeles (1980-82), D.Sc. in applied math (1987); worked at University of Florida; Max-Planck-Institute, Munich, Germany, Kyushu Institute of Technology, Meiji and Rikkyo University in Japan, and several other institutions. He is on the editorial board of IEEE TNN, CPC, NIP-LR, Journal of Mind and Behavior, and 7 other journals; co-founder & scientific editor of the "Polish Cognitive Science" journal; president of the European Neural Networks Society (2006-2008), member of IEEE NNS Technical committee; expert of the European Union science programs; published over 350 scientific and popular articles, 4 books, edited many others, his DuchSoft company makes GhostMiner software package marketed by Fujitsu. Expert in computational intelligence (CI), especially methods that facilitate understanding of data, and algorithms inspired by models of brain functions at different levels. Among other topics s on creation of general CI theory based on similarity evaluation, meta-learning schemes that automatically discover the best model for a given data, geometrical theories for modeling of mental events and relating such models to neurodynamics, and toys that facilitate mental development. With a wide background in many branches of science and understanding of different cultures he bridges various scientific communities. As a service to the international community maintains many web pages related to CI, computational neuroscience, machine learning and statistics. To access these pages and his full CV type "Duch" in Google.

Fault Tolerant Systems Design in VLSI using Data Compression under Constraints of Failure Probabilities – Overview and Status

Professor Sunil R. Das

School of Information Technology and Engineering, Faculty of Engineering
University of Ottawa, Ottawa, Ontario K1N 6N5, Canada
and

Department of Computer and Information Science, College of Arts and Sciences
Troy University, Montgomery, AL 36103, U. S. A.

Abstract: The realization of space-efficient support hardware for built-in self-testing (BIST) is of critical importance in the design and manufacture of VLSI circuits. Novel approaches to designing aliasing-free space compaction hardware were recently proposed in the context of testing cores-based system-on-chip (SOC) for single stuck-line faults, extending the well-known concepts of conventional switching theory, specifically those of cover table and frequency ordering commonly utilized in the simplification of switching functions, and of compatibility relation as used in the minimization of incomplete sequential machines, based on optimal generalized sequence mergeability, as developed and utilized by the author and his coworkers in earlier works.

Embedded cores-based design paradigm has evolved from the necessity to increase design productivity and decrease time-to-market, but as a result has created numerous challenging problems for the test design community. Keeping in view the many formidable issues that arise in testing these cores-based SOCs, this lecture will provide a brief overview on the general methodology of built-in self-test (BIST) in the context of embedded cores-based system chips, as is widely used in today's many commercial products with remarkable success, emphasizing the basic philosophy of the technique, test pattern generation procedures, output compaction schemes, test implementation and evaluation methods, with impact on a wide spectrum of issues facing the testing community at the moment.

Also, with details of the different algorithms developed in the implementation of the approaches to designing zero-aliasing space compactors, the lecture will provide the mathematical basis of selection criteria for merger of an optimal number of outputs of the CUT to achieve maximum compaction ratio in the design, along with some results from simulation experiments conducted on ISCAS 85 combinational and ISCAS 89 full-scan sequential benchmark circuits, with simulation programs ATALANTA, FSIM, and HOPE.

Brief Biography of the Speaker:

Sunil R. Das (M'70-SM'90-F'94-LF'04) is an Emeritus Professor of Electrical and Computer Engineering at the School of Information Technology and Engineering, University of Ottawa, Ottawa, ON, Canada and a Professor of Computer and Information Science, Troy University, Montgomery, AL, USA. He holds a B.Sc. (Honors) in Physics and an M.Sc. (Tech) and a Ph.D. in Radiophysics and Electronics from the University of Calcutta, Calcutta, West Bengal, India. He previously held academic and research positions with the Department of Electrical Engineering and Computer Sciences, Computer Science Division, University of California, Berkeley, CA, the Center for Reliable Computing (CRC), Computer Systems Laboratory, Department of Electrical Engineering, Stanford University, Stanford, CA (on

sabbatical leave), the Institute of Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, ROC, and the Center of Advanced Study (CAS), Institute of Radiophysics and Electronics, University of Calcutta.

Dr Das has published around 300 papers in the areas of switching and automata theory, digital logic design, threshold logic, fault-tolerant computing, built-in self-test with emphasis on embedded cores-based system-on-chip (SOC), microprogramming and microarchitecture, microcode optimization, applied theory of graphs, and combinatorics. He served in the Technical Program Committees and Organizing Committees of many IEEE and non-IEEE International Conferences, Symposia, and Workshops, and also acted as session organizer, session chair, and panelist.

Dr Das was elected one of the delegates of the prestigious GOOD PEOPLE, GOOD DEEDS of the Republic of China in 1981 in recognition of his outstanding contributions in the field of research and education. He is listed in the MARQUIS WHO'S WHO Biographical Directory of the Computer Graphics Industry, Chicago, IL (First Edition, 1984).

Dr Das served as the Managing Editor of the IEEE VLSI Technical Bulletin, a publication of the IEEE Computer Society Technical Committee (TC) on VLSI since its very inception, and also was an Executive Committee Member of the IEEE Computer Society Technical Committee (TC) on VLSI. Dr Das also served as an Associate Editor of the IEEE Transactions on Systems, Man, and Cybernetics (subsequently Part A, Part B, and Part C) since 1991 until very recently. He is currently an Associate Editor of the IEEE Transactions on Instrumentation and Measurement, an Associate Editor of the International Journal of Computers and Applications published by Acta Press, Calgary, AB, a Regional Editor for Information Technology Journal, an official publication of Asian Network for Scientific Information, and a former Member of the Editorial Board and a Regional Editor for Canada of the VLSI Design: An International Journal of Custom-Chip Design, Simulation and Testing published by Gordon and Breach Science Publishers, Inc., NY. Dr Das is a former Administrative Committee (ADCOM) Member of the IEEE Systems, Man, and Cybernetics Society, a former Associate Editor of the IEEE Transactions on VLSI Systems (for two consecutive terms), a former Associate Editor of the SIGDA Newsletter, the publication of the ACM Special Interest Group on Design Automation, a former Associate Editor of the International Journal of Computer Aided VLSI Design published by Ablex Publishing Corporation, Norwood, NJ, and a former Associate Editor of International Journal of Parallel and Distributed Systems and Networks published by Acta Press. Dr Das also served as the Co-Chair of the IEEE Computer Society Students Activities Committee from Region 7 (Canada). He was the Associate Guest Editor of the IEEE Journal of Solid-State Circuits Special Issues on Microelectronic Systems (Third and Fourth Special Issues), and Guest Editor of the International Journal of Computer Aided VLSI Design (September 1991) as well as VLSI Design: An International Journal of Custom-Chip Design, Simulation and Testing (March 1993, September 1996, and December 2001), Special Issues on VLSI Testing. He also Guest Edited jointly with Rochit Rajsuman Special Sections of the IEEE Transactions on Instrumentation and Measurement in the area of VLSI Testing, first in October 2003 (Innovations in VLSI Test Equipments), and then in October 2005 and April 2006 (Future of Semiconductor Test). Dr Das is the founding Editor-in-Chief of the International Journal of Computers, Information Technology and Engineering being published by Serials Publications, Delhi, India.

Dr Das edited jointly with P. K. Srimani a book entitled, Distributed Mutual Exclusion Algorithms, published by the IEEE Computer Society Press. Los Alamitos, CA 1992 in its Technology Series. He is also the author jointly with C. L. Sheng of a text on Digital Logic Design to be published by Ablex Publishing Corporation.

Dr Das is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), Inc. (with separate membership in the IEEE Computer Society, IEEE Systems, Man, and Cybernetics Society, IEEE Circuits and Systems Society, and IEEE Instrumentation and Measurements Society), and a Member of the Association for Computing Machinery (ACM), U.S.A. He was elected a Fellow of the IEEE in 1994 for contributions to switching theory and computer design.

Dr Das is the 1996 recipient of the IEEE Computer Society's highly esteemed Technical Achievement Award for his pioneering contributions in the fields of switching theory and modern digital design, digital circuits testing, microarchitecture and microprogram optimization, and combinatorics and graph theory. He is also the 1997 recipient of the IEEE Computer Society's Meritorious Service Award for excellent service contributions to IEEE Transactions on VLSI Systems and the Society, and was elected a Fellow of the Society for Design and Process Science, U.S.A. in 1998 for his accomplishments in integration of disciplines, theories and methodologies, development of scientific principles and methods for design and process science as applied to traditional disciplines of engineering, industrial leadership and innovation, and educational leadership and creativity. In recognition as one of the distinguished core of dedicated volunteers and staff whose leadership and services made the IEEE Computer Society the world's preeminent association of computing professionals, Dr Das was made a Golden Core Member of the Computer Society in 1998. Besides, Dr Das is the recipient of the IEEE Circuit and Systems Society's Certificates of Appreciation for services rendered as Associate Editor, IEEE Transactions on Very Large Scale Integration Systems, during 1995-1996 and during 1997-1998, and of the IEEE Computer Society's Certificates of Appreciation for services rendered to the Society as Member of the Society's Fellow Evaluation Committee, once in 1998 and then in 1999. Dr Das served as a Member of the IEEE Computer Society's Fellow Evaluation Committee for 2001 as well. He was elected a Fellow of the Canadian Academy of Engineering in 2002 for pioneering contributions to computer engineering research – specifically in the fields of switching theory and computer design, fault-tolerant computing, microarchitecture and microprogram optimization, and to some problem areas in applied theory of graphs and combinatorics. Dr Das was elected a Fellow of the Engineering Institute of Canada in 2005 for exceptional contributions to Engineering to Canada.

Dr Das is the recipient of the prestigious Rudolph Christian Karl Diesel Best Paper Award of the Society for Design and Process Science in recognition of the excellence of their paper presented at the Fifth Biennial World Conference on Integrated Design and Process Technology held in Dallas, TX during June 4-8, 2000. He is also the co-recipient of the IEEE's esteemed Donald G. Fink Prize Paper Award for 2003 for their paper published in the December 2001 issue of the IEEE Transactions on Instrumentation and Measurement.

Modeling and Analysis of the Web-Like Networks

Professor Narsingh Deo
Nanjing Normal University
Nanjing, Jiangsu, China

Abstract: With the dramatic growth of the World Wide Web (Web) and the Internet, the study of large, random networks has acquired new prominence. Recent empirical studies have shown statistical similarities between these two and other complex, real-life networks such as the network of phone calls, power-distribution networks, citation network, science-collaboration network, movie-actor collaboration network, neural networks, and various infrastructure networks. The ubiquity and the increasing importance of such networks have spawned a truly cross-disciplinary research aimed at understanding their fundamental properties and functions.

Viewed as large, random graphs in which birth and death of nodes and links are taking place continuously, these graphs differ from the classical Erdos-Renyi random graphs in significant ways. Some of these differences have recently been discovered through empirical studies of the real-life networks; a great deal more remains to be discovered. In this talk we will present an overview of recently-proposed (by us and others) dynamic random graph models of these complex, large, real-life networks in a unified manner; explain salient techniques (graph-theoretic, statistical, and computational) used in analyzing these models; and discuss the main results derived through these techniques. For instance, how the structural properties of social networks facilitate or impede the spread of diseases, or how the properties of the Internet can be exploited to devise efficient strategies for containing the spread of viruses and worms.

Brief Biography of the Speaker:

Professor Narsingh Deo is known for his work in computational graph theory and in parallel algorithms. He holds the Charles N. Millican Eminent Scholar's Chair in Computer Science and is the Director of the Center for Parallel Computation at University of Central Florida, Orlando. Prior to this, he was a Professor of Computer Science at Washington State University, where he also served as the department chair. Before that he was a Professor of Electrical Engineering and Computer Science at the Indian Institute of Technology, Kanpur, and a Member of Technical Staff at Jet Propulsion Laboratory. He has a Ph.D. from Northwestern University, an MS from Caltech and an undergraduate degree from Indian Institute of Science—all in Electrical Engineering.

He has held Visiting professorships at numerous institutions—including at the University of Illinois, Urbana; University of Nebraska, Lincoln; Indian Institute of Science, Bangalore; and IBM's T. J. Watson Research Center, ETH, Zurich, University of Sao Paulo, Brazil, Oak Ridge National Lab., Australian National University, Canberra, Chuo University, Tokyo, and IIT/Kharagpur.

A Fellow of the IEEE, a Fellow of the ACM, and Fellow of the ICA, Dr. Deo has authored four books and about 200 refereed research papers. He holds a number of patents in computer hardware and is a recipient of NASA's Apollo Achievement Award. Among his other awards are: Gold Medal of Patna University; Drake Scholar at Caltech Governor's Award for Outstanding Contribution to High Tech Research in Florida (1989); UCF's Distinguished Researcher Award-89; UCF's Professorial Excellence Program Award (1997); UCF's Teaching Incentive Program Award

(1999); and UCF's Excellence in Graduate Teaching Award (2001). He has served as an editor/guest editor/ member of the editorial board for various journals--including the IEEE Trans. on Circuits & Systems, the Journal for Parallel and Distributed Computing; the Journal of Supercomputing, and the VLSI Design Journal. He is currently the president of the Forum for Interdisciplinary Mathematics.

The Impact of Open Educational Resources, Web 2.0, and XML on Education

Professor C. Sidney Burrus
Rice University, Houston
Texas, USA

Abstract: Web 2.0 and XML are the basis of the next generation of the World Wide Web. One of the areas of greatest impact will be education. The current web and HTML have been on the first phase of impact by giving a picture of information. The adding of metadata through XML is the second phase which will allow "knowledge" as well as information to be encoded in a document and make documents more machine readable as well as human readable. Teachers and educators are only beginning to think about how to use this but it has the potential of being the largest paradigm shift in the history of teaching. Examples of the use in mathematics, chemistry, and music will be given with speculation on other areas.

The Open Educational Resource (OER) movement was inspired by the Open Source movement in computer software development. If a common format such as XML and a common (or compatible) copyright license is used, communities of authors, teachers, and learners come into being in a new way. They are productive in completely new way. GNU/Linux, Wikipedia, Connexions, QOOP, Creative Commons, GPL, OSI, Teachers without Borders, etc. are examples of that. The coupling of educational material encoded in XML and available on the web with the Creative Commons copyright system will not only revolutionize education but the publication industry that feeds the current system.

Brief Biography of the Speaker:

C. Sidney Burrus is Research Professor of Electrical and Computer Engineering at Rice University. He received his PhD from Stanford University, was Dean of Engineering at Rice from 1998 to 2005, Director of the Computer and Information Technology Institute from 1992 to 1998, and Chair of the ECE Department from 1984 to 1992. He is a Fellow of the IEEE, has received various teaching awards from Rice, various research awards from IEEE and others, has written 5 books and published over 200 articles on Digital Signal Processing (DSP), and was a visiting faculty member at MIT and at the University of Erlangen in Germany. He was a member of the founding committee for the new International University Bremen in Germany. Recently, he has been involved with the use of technology in education and in eLearning. He has been on the board of Connexions since it was founded in 1999 and is now Strategist for Connexions.

Design Challenges and Opportunities of the “End of Scaling” Nanoscale CMOS

Professor Ching-Te Chuang
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Abstract: This presentation reviews the challenges and opportunities of high-performance digital design in the “End of Scaling” nanoscale CMOS technologies. The device structure evolution, material enhancement, and major design challenges are discussed. Examples of logic circuit and SRAM design techniques to overcome the challenges and to mitigate various performance/reliability constraints in conventional planar CMOS technology are given. Scaled/emerging technologies such as scaled PD/SOI, UT/SOI, strained-Si channel device, hybrid orientation technology, and multi-gate FinFET are addressed with particular emphases on the implications and impacts on circuit design. Finally, novel logic circuit, SRAM, and power-gating schemes exploiting unique structures and properties of emerging devices are discussed.

Brief Biography of the Speaker:

Dr. Chuang received the B.S.E.E. from National Taiwan University, Taipei, Taiwan in 1975 and Ph.D. degree in Electrical Engineering from University of California, Berkeley, CA in 1982.

He joined the IBM T. J. Watson Research Center, Yorktown Heights, NY in 1982, and is currently Manager of the High-Performance Circuit Group. Since 1993, his group has been primarily responsible for the circuit design of IBM’s high-performance CMOS microprocessors for enterprise servers, PowerPC workstations, and game/media processors. Since 1996, he has been leading the efforts in evaluating and exploring scaled/emerging technologies, such as PD/SOI, UT/SOI, strained-Si devices, hybrid orientation technology, and multi-gate/FinFET devices, for high-performance logic and SRAM applications.

Dr. Chuang is a Fellow of IEEE. He has authored or coauthored over 250 papers. He holds 21 U.S. patents with another 19 pending.

Artificial MetaPlasticity and the Challenge to train ANNS with reduced Pattern Availability

Professor Diego Andina
Head of Group for Automation in Signals and Communications (GASC)
Technical University of Madrid (UPM)
SPAIN

Abstract: Artificial implementation of Biological Metaplasticity property of synapses has been recently proposed by the author to improve Artificial Neural Networks (ANN) design. This upgrade of existing models claims a much more efficient information extraction from the patterns available to train the ANN. The hypothesis has been tested as an application example in the Multilayer Perceptron (MLP) case, probably the most widely ANN applied through the ANN history. The results show a

much more efficient training that is of crucial relevance when few training patterns are the only information font for the ANN design.

Brief Biography of the Speaker:

Diego Andina is Master in Computer Science and Communications simultaneously and with Honors by Technical University of Madrid (UPM) in 1990 and also the Ph D. degree "cum laude" by Technical University of Madrid in 1995. Presently is Head of Group for Automation in Signals and Communications (GASC), Technical University of Madrid, UPM, Spain.

His research interests are: Signal Processing & Communications Theory (including the internet end e-commerce) combined with Soft Computing techniques as Artificial Neural Networks, Fuzzy Logic, Genetic Algorithms, Adaptive Nonlinear Systems, etc. Author of more than 100 national and international publications, he has been director of more than 30 Research projects financed by National Government, European Commission or Private Institutions and Firms. He is also Associate Editorial Member of several International Journals and Transactions and has participated in the organization of more than 35 international events He is Founder and Director of the European Latino American Cooperation for Intelligent Automation and Control Network (ELACIAC International Research Network), officially recognized by the European Commission.

Discrete Optimization Methods, the Ameso Class of Problems and their Applications in Logistics and Supply Chains

Professor Michael N. Katehakis

Management Science & Information Systems
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180 University Avenue
Newark Nj 07010
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Abstract: In this talk we will survey methods of discrete optimization used in areas such as optimal in process operations, logistics, supply chain management, planning and scheduling.

We will review the major recent developments in mixed-integer linear, nonlinear programming and decomposition techniques for solving these problems.

We will next discuss a new class of discrete optimization problems the $\{\backslashsl\ ameso\}$ programming problems. We show that:

- i) for the one dimensional ameso optimization problems there are simple, to verify, optimality conditions at any optimal point,
- ii) one can define the conditional pair of an ameso($\$C\$$) pair and this is also an ameso($\$C\$$) pair,
- iii) (i) and (ii) can be used to construct a procedure that solves ameso optimization problems without necessarily performing complete enumeration.

We will present several applications for logistics planning and scheduling to illustrate the models and methods discussed in this talk.

Brief Biography of the Speaker:

Professor Katehakis is a well known authority on Dynamic Programming and Applied Probability. His work has been published in a variety of professional journals including Probability in the Engineering and Information Sciences, Annals of Applied Probability, Advances in Applied Probability, Management Science, Mathematics of Operations Research, Advances in Applied Mathematics, and the Proceedings of the National Academy of Sciences U.S.A. He is the winner of the 1992 Wolfowitz Prize. He is a member of the editorial boards of the American Journal of Mathematical and Management Sciences, The Naval Research Logistics and the Journal of Probability in the Engineering and Informational Sciences. In the USA he has taught at several well known Universities including Rutgers the State University of New Jersey, Columbia University, Stanford University and the State University of New York at Stony Brook. In Greece he has taught at the University of Crete, Heraklion, University of Athens and the Polytechnic of Crete at Chania.

He received many honors and awards and is included in the "Who's Who Among American Teachers & Educators" Registry.

Professor Katehakis holds a Ph.D. from Columbia University in Operations Research, an M.A. from the University of South Florida in Mathematics, an M.S from Columbia University in Mathematical Methods in Engineering and Operations Research, 1976. and a Diploma from the University of Athens Greece.

We would like to thank all members of the organizing laboratories for their contribution to the organization of the conference.

The contents of this Book are also published in the CD-ROM Proceedings of the Conference. Both will be sent to the WSEAS collaborating indices after the conference: www.worldses.org/indexes.

In addition, papers of this book are permanently available to all the scientific community via the WSEAS E-Library.

Expanded and enhanced versions of papers published in these conference proceedings are also going to be considered for possible publication in one of the WSEAS journals that participate in the major International Scientific Indices (Elsevier, Scopus, EI, Compendex, INSPEC, CSA see: www.worldses.org/indexes) these papers must be of high-quality (break-through work) and a new round of a very strict review will follow. (No additional fee will be required for the publication of the extended version in a journal).

We cordially thank all the people of WSEAS for their efforts to maintain the high scientific level of conferences, proceedings and journals.

The Editors

**PROCEEDINGS OF the 6th WSEAS International Conference on
COMPUTATIONAL INTELLIGENCE, MAN-MACHINE SYSTEMS
and CYBERNETICS (CIMMACS '07)
TABLE OF CONTENTS**

The Minimum Distance of the Dual of a CRC <i>H. D. Wacker, J. Boercsoek</i>	1
Optimal Strategy for Control a Pilot Plant Reactor <i>Paulo Salgado, Paulo Afonso, Manuela Cunha</i>	6
Optimization of Control of Unmanned Underwater Vehicle in Collision Situation <i>Bogdan Zak</i>	12
Analytically Tuned Parameters of Simulated Annealing for the Timetabling Problem <i>Juan Frausto-Solis, Federico Alonso-Pecina, Cinhtia Gonzalez-Segura</i>	18
Behaviour Patterns Evolution on Individual and Group Level <i>Stanislav Slusny, Roman Neruda, Petra Vidnerova</i>	24
Neural Network Boolean Factor Analysis and Application <i>Dusan Husek, Alexander Frolov, Pavel Polyakov, Vaclav Snasel</i>	30
Particle Swarm Optimization for the Continuous p-Median Problem <i>Julio Brito, Francisco J. Martinez, Jose A. Moreno</i>	36
Swarm Intelligence and its Applications in Swarm Robotics <i>Aleksandar Jevtic, Diego Andina</i>	42
Greater Knowledge Extraction Based on Fuzzy Logic and GKPFM Clustering Algorithm <i>Benjamin Ojeda-Magana, Ruben Ruelas, Fulgencio S. Buendia Buendia, Diego Andina</i>	48
Modeling the Calcium Dysregulation Hypothesis of Alzheimer's Disease <i>Julio Monteiro, Marcio Lobo Netto, Diego Andina, Javier Roper Pelaez</i>	53
Artificial MetaPlasticity and the Challenge to Train ANNS with Reduced Pattern Availability <i>Diego Andina</i>	58
Multiple Faces Detection in Real Time using Neural Networks <i>Stephen Karungaru, Minoru Fukumi, Takuya Akashi, Norio Akamatsu</i>	64
A Comparison of Soft Fusion Methods under Different Bagging Scenarios <i>Fuad Alkoot, Hussain Qasem</i>	70
MaculaTEST - Computer Aided Diagnosis System for Macular Diseases <i>Marius Cristian Luculescu, Simona Lache</i>	78
Monitoring System of Assisted Movement of Visually Impaired <i>V. Tiponut, D. Ianchis, Z. Haraszy, S. Popescu</i>	84
Soft Computing Technique in Prediction of Pavement Condition <i>Devinder Kaur, Debargha Datta</i>	88
Parallelization of Prime Number Generation Using Message Passing Interface <i>Izzatdin Aziz, Nazleeni Haron, Low Tan Jung, Wan Rahaya Wan Dagang</i>	94

Computational Efficient Implementation of the Second Order Volterra Filter Based on the MMD Approximation <i>Georgeta Budura, Corina Botoca</i>	99
A Novel Hybrid Algorithm for Join Ordering Problem in Database Queries <i>Ali Safari Mamaghani, Kayvan Asghari, Fariborz Mahmoudi, Mohammad Reza Meybodi</i>	105
Ships Classification using Hydroacoustic Signatures <i>Andrzej Zak</i>	111
Trajectory Based Hand Gesture Recognition <i>Daniel Popa, Georgiana Simion, Vasile Gui, Marius Ottesteanu</i>	116
Minimum Description Length Characterization of Low End Color Cameras <i>Adrian Burian, Mihaela Cirlugea</i>	122
Target Detection in Low Visibility Condition and Artificial Lighting Using a Laser Sensor <i>Georgiana Simion, Marius Ottesteanu, Aurel Gontean</i>	126
Barley Seeds Classification with a Genetically Optimized Kernel Density Estimator <i>Vasile Gui, Florin Alexa, Catalin Căleanu</i>	131
A New Point Matching Method for Image Registration <i>Daniela Fuiorea, Vasile Gui, Florin Alexa, Corneliu Toma</i>	135
Considerations on Acoustic Source Localization <i>Lucian Jurca, Aurel Gontean, Ioan Jivet, Benjamin Dragoi</i>	140
Evaluation of Training Methods for Conditioning of Fuzzy Based Maintainability Metric <i>Jitender Kumar Chhabra, Surender Singh Dahiya, Shakti Kumar</i>	146
Wireless Communication Techniques for Home Automation Sensors <i>Ciprian Seiculescu, Ioan Lie, Aurel Gontean</i>	152
Development of a GPS-Based Autonomous Water Pollution Monitoring System Using Fish Robots <i>Daejung Shin, Seung Y. Na, Jin Y. Kim, Seong-Joon Baek, Mingyu Song, Aaron Park</i>	157
A Flexible Neural Network for ATM Cash Demand Forecasting <i>Rimvydas Simutis, Darius Dilijonas, Lidija Bastina, Josif Friman</i>	163
A Direct Digital Synthesis Firmware Development Framework <i>I. Jivet, B. Dragoi, M. Ottesteanu, L. Jurca</i>	167
An Improved Snake for Automatic Building Extraction <i>Lau Bee Theng, Raymond Chiong</i>	172
Fuzzy Model for Estimation of Passenger Car Unit <i>Praveen Aggarwal</i>	178
Voltage Control Study Using UPFC Based on Biological Computing Optimization Technique <i>Nur Dianah Mohd. Radzi, Ismail Musirin, Mohamad Khayat Idris, Abdul Rahman Minhat, Muhammad Murtadha Othman</i>	187
Fuzzy Control of Motion of Underwater Robotic Vehicle <i>Jerzy Garus</i>	193
Classification Model based on Rough and Fuzzy Sets Theory <i>Pavel Jirava, Jiri Krupka</i>	199

Retail Banking Optimization System based on Multi-Agents Technology <i>Darius Dilijonas, Lidija Bastina</i>	204
Influence of the Rail-to-Rail Feature of the Operational Amplifier on the Performance of an Instrumentation System <i>Alvaro Llaria, Octavian Curea, Jaime Jimenez</i>	210
Determination of Available Transfer Capability (ATC) Considering Integral Square Generator Angle (ISGA) <i>N. Mat, M. M. Othman, I. Musirin, A. Mohamed, A. Hussain</i>	215
Feasibility of One-Class-SVM for Anomaly Detection in Telecommunication Network <i>Shaoyan Zhang, Rui Zhang, Sethuraman Muthuraman, Jianmin Jiang</i>	221
Energy Aware HW/SW Integration in an Autonomous Microrobot <i>A. Sanuy, R. Casanova, M. Szymanski, H. Worn, J. Samitier, A. Dieguez</i>	226
A Framework Model through Data Flow Diagrams to Model an Air Traffic Control System <i>D. M. Akbar Hussain, M. Z. Khan, Z. Ahmed, K. Ahmad, S. Majeed, M. A. Malik</i>	232
OPC for Process Maintenance <i>M. H. Schwarz, J. Boercsoek</i>	238
A New Version of the Flusser Invariants Set for Pattern Feature Extraction <i>Constantin-Iulian Vizitiu, Doru Munteanu</i>	245
Robust Romanian Language Automatic Speech Recognizer <i>Doru-Petru Munteanu, Constantin-Iulian Vizitiu</i>	251
An Overview of System Dynamics Methods for Developing Management Flight Simulators <i>George Papageorgiou, Kristina Abrosimova</i>	255
Muscle Force Estimation using a Measure of Muscle Activation Extracted from Surface EMG <i>Rok Istenic, Ales Holobar, Marco Gazzoni, Damjan Zazula</i>	261
An Improved Quadtree-Based Algorithm for Lossless Compression of Volumetric Datasets <i>Gregor Klajnsek, Bojan Rupnik, Denis Spelic</i>	265
Fuzzy Clustering Based Models for Supervision of Industrial Processes <i>Miguel Ramirez, Eliezer Colina</i>	272
A Hybrid Simulated Annealing and Threshold Accepting for Satisfiability Problems using Dynamically Cooling Schemes <i>Felix Martinez-Rios, Juan Frausto-Solis</i>	282
Control of Complex Machines for Meta-Learning in Computational Intelligence <i>Krzysztof Grabczewski, Norbert Jankowski</i>	287
Learning Data Structures with Inherent Complex Logic: Neurocognitive Perspective <i>Wlodzislaw Duch</i>	294
Efficient Protection Against Data Errors in Embedded Control Software <i>Michael Short, Michael Schwarz, Josef Boercsoek</i>	304
Hybrid Mirrors for Driving Simulators – Design, Construction and Experiments <i>Stanislav Novotny, Petr Bouchner, Roman Peknik, Jan Pekny, Vaclav Jirkovsky, Martin Kozumplik</i>	310
LOPA – A Method to Analyse Safety Integrity Systems according to IEC 61511 <i>P. Holub, J. Borcsok</i>	316

Digital Trimulus Color Image Enhancing and Quantitative Information Measuring <i>Zhengmao Ye, Habib Mohamadian, Yongmao Ye</i>	324
Fault Tolerant Systems Design in VLSI Using Data Compression Under Constraints of Failure Probabilities – Overview and Status <i>Sunil R. Das</i>	330
Intelligent System Facilitating Service Selection <i>Sylvia Encheva, Sharil Tumin</i>	339
ANN/DT Approach for Security Evaluation and Preventive Control of Power Systems <i>M. K. Shah, K. R. Niazi, C. M. Arora</i>	342
Representative Pattern Extraction for Nucleotide Sequence Groups Using Base Frequency Differences <i>Kyoung Soon Hwang, Keon Myung Lee, Sung Soo Kim, Chan-Hee Lee, Hyung Woo Yoon, Sung Duk Lee</i>	349
MASDScheGATS: A Prototype System for Dynamic Scheduling <i>Ana Madureira, Joaquim Santos, Ivo Pereira</i>	354
Special Semi-Supervised Techniques for Natural Language Processing Tasks <i>Richard Farkas, Gyorgy Szarvas, Janos Csirik</i>	360
Markov Models for 2004 Architecture for Safety Related Systems <i>Josef Borcsok, Evzudin Ugljesa</i>	366
Automated System for DMM Calibration <i>Vladislav Slavov, Tasho Tashev, Valeri Mladenov</i>	372
Data Mining : As an Imperative Tool for Discovering Knowledge <i>Anoop K. Paharia, Yachana Bhawsar, Divakar Singh</i>	376
Developing Web intelligence using Data Mining <i>Anoop Paharia, Yachana Bhawsar, Divakar Singh</i>	380

Authors Index

Abrosimova, K.	255			Grabczewski, K.	287			Munteanu, D.	245	251
Afonso, P.	6			Gui, V.	116	131	135	Musirin, I.	215	
Aggarwal, P.	178			Haraszy, Z.	84			Musirin, I.	187	
Ahmad, K.	232			Haron, N.	94			Muthuraman, S.	221	
Ahmed, Z.	232			Holobar, A.	261			Na, S. Y.	157	
Akamatsu, N.	64			Holub, P.	316			Neruda, R.	24	
Akashi, T.	64			Husek, D.	30			Netto, M.	53	
Hussain, D.M.	232			Hussain, A.	215			Niazi, K. R.	342	
Alexa, F.	131	135		Hwang, K.	349			Novotny, S.	310	
Alkoot, F.	70			Ianchis, D.	84			Ojeda-Magana, B.	48	
Alonso-Pecina, F.	18			Idris, M.	187			Otesteanu, M.	167	
Andina, D.	42	48		Istenic, R.	261			Otesteanu, M.	116	126
Andina, D.	53	58		Jankowski, N.	287			Othman, M.	187	
Arora, C. M.	342			Jevtic, A.	42			Othman, M.M.	215	
Asghari, K.	105			Jiang, J.	221			Paharia, A.	376	380
Aziz, I.	94			Jimenez, J.	210			Papageorgiou, G.	255	
Baek, S. J.	157			Jirava, P.	199			Park, A.	157	
Bastina, L.	163	204		Jirkovsky, V.	310			Peknik, R.	310	
Bhawsar, Y.	376	380		Jivet, I.	167			Pekny, J.	310	
Borcsok, J.	316	1	238	Jivet, I.	140			Pelaez, J.	53	
Borcsok, J.	304	366		Jung, L.	94			Pereira, I.	354	
Botoca, C.	99			Jurca, L.	167			Polyakov, P.	30	
Bouchner, P.	310			Jurca, L.	140			Popa, D.	116	
Brito, J.	36			Karungaru, S.	64			Popescu, S.	84	
Budura, G.	99			Kaur, D.	88			Qasem, H.	70	
Buendia, F. S.	48			Khan, M. Z.	232			Radzi, N. D.	187	
Burian, A.	122			Kim, J. Y.	157			Ramirez, M.	272	
Caleanu, C.	131			Kim, S. S.	349			Ruelas, R.	48	
Casanova, R.	226			Klajnsek, G.	265			Rupnik, B.	265	
Chhabra, J. K.	146			Kozumplik, M.	310			Salgado, P.	6	
Chiong, R.	172			Krupka, J.	199			Samitier, J.	226	
Cirlugea, M.	122			Kumar, S.	146			Santos, J.	354	
Colina, E.	272			Lache, S.	78			Sanuy, A.	226	
Csirik, J.	360			Lee, Ch.	349			Schwarz, M.	304	
Cunha, M.	6			Lee, K.	349			Schwarz, M. H.	238	
Curea, O.	210			Lee, S. D.	349			Seiculescu, C.	152	
Dahiya, S. S.	146			Lie, I.	152			Shah, M. K.	342	
Das, S. R.	330			Llaria, A.	210			Shin, D.	157	
Datta, D.	88			Luculescu, M.	78			Short, M.	304	
Dieguez, A.	226			Madureira, A.	354			Simion, G.	116	126
Dilijonas, D.	163	204		Mahmoudi, F.	105			Simutis, R.	163	
Dragoi, B.	167	140		Majeed, S.	232			Singh, D.	376	380
Duch, W.	294			Malik, M. A.	232			Slavov, V.	372	
Encheva, S.	339			Malik, M. A.	232			Slusny, S.	24	
Farkas, R.	360			Mamaghani, A.	105			Snasel, V.	30	
Frausto-Solis, J.	18	282		Martinez, F. J.	36			Song, M.	157	
Friman, J.	163			Martinez-Rios, F.	282			Spelic, D.	265	
Frolov, A.	30			Mat, N.	215			Szarvas, G.	360	
Fuiorea, D.	135			Meybodi, M.	105			Szymanski, M.	226	
Fukumi, M.	64			Minhat, A.	187			Tashev, T.	372	
Garus, J.	193			Mladenov, V.	372			Theng, L.	172	
Gazzoni, M.	261			Mohamadian, H.	324			Tiponut, V.	84	
Gontean, A.	126	140	152	Mohamed, A.	215			Toma, C.	135	
Gonzalez-Segura, C.	18			Monteiro, J.	53			Tumin, S.	339	
				Moreno, J. A.	36					

Authors Index

Ugljesa, E.	366		Woo Yoon, H.	349	Zak, B.	12
Vidnerova, P.	24		Worn, H.	226	Zazula, D.	261
Vizitiu, C. L.	245	251	Ye, Y.	324	Zhang, R.	221
Wacker, H. D.	1		Ye, Z.	324	Zhang, S.	221
Wan Dagang, W. R.	94		Zak, A.	111		